Resiliency Challenges in Future Communications Infrastructure

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Outline

NFVI and desired Characteristics
The Resiliency Challenge
Faults, Effects, and Measures
Resiliency framework for NFV
Summary
Infrastructural Challenges

New kinds of consumers
5 Billion
people will be directly touched by connectivity in 2015

New kinds of devices
55%
of respondents say their next phone purchase will be a smartphone

New kinds of connections
29X
is the amount that mobile data connectivity will grow between 2010 and 2015

New ecosystems
$46 Billion
in revenue will be generated worldwide by consumer mobile apps in 2015

Source: Yankee Group*, 2012

*Other names and brands may be claimed as the property of others.
Transforming the Network with SDN and NFV

Traditional Networking

SDN

Mobility Management Element (MME)  Packet Data Network Gateway (PDN)  Serving Gateway (SGW)  VM: MME  VM: PDN  VM: SGW  SDN/NFV
NFV End User Value Proposition

Lower TCO  On-Demand Service  Rapid Service Innovation
NFV Infrastructure Attributes

Reliability
Availability
Manageability
Security
Performance

RAS → A main theme
Increasingly Common Faults

Faults can be very costly
Moore’s Law

# Transistors double every ~2 years

Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.
Unprecedented Integration

• Moore’s Law enables unprecedented levels of integration
• Heterogeneous system integration of Cores, Graphics, Media, IOs, memory technologies, etc. to satisfy USERS’ experiences and reduce OPERATORS’ expenditures

Heterogeneous System Integration further drives the Resiliency Challenge
Potential Fault Sources

- Transistors
- Sockets
- Voltage
- Packaging
- Cores
- Integration
# Types of Faults

<table>
<thead>
<tr>
<th>Faults</th>
<th>Type</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Permanent faults</td>
<td>Stuck at 0 - 1</td>
<td>Open, shorts, power supply or fan shutdown</td>
</tr>
<tr>
<td>Gradual faults</td>
<td>Spatial: Variations</td>
<td>Fast and slow cores</td>
</tr>
<tr>
<td></td>
<td>Temporal: Temperature effects</td>
<td>Change in frequency with temperature</td>
</tr>
<tr>
<td>Aging faults</td>
<td>Degradation (slow gradual temporal)</td>
<td>Loss of frequency over time, erratic bits in memory</td>
</tr>
<tr>
<td>Intermittent/transient faults</td>
<td>Soft errors (radiation induced)</td>
<td>Flipped bit causes data corruption, loss of control, not reproducible</td>
</tr>
</tbody>
</table>

## Faults cause errors (data & control)

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<tbody>
<tr>
<td>Datapath/array errors</td>
<td>Detected/corrected by parity/ECC</td>
</tr>
<tr>
<td>Control errors</td>
<td>Control lost (Blue screen. system hang)</td>
</tr>
<tr>
<td>Silent Data Corruption</td>
<td>Not detectable</td>
</tr>
</tbody>
</table>
Sources of Variations

Random Dopant Fluctuations

Heat Flux (W/cm²)—Vcc variation

Sub-wavelength Lithography

Temp Variation & Hot spots

Source: Mark Bohr, Intel
Variability and Degradation

Smaller Transistors
Higher $\sigma$ in $V_t$
$\sim 10$ mV in $\sigma(V_t)$ per generation

Transistor aging
Degrades drive current with time
Results in performance loss over time

Source: Jose Maiz, Intel
When designed to voltage scale

Energy Efficiency

Freq

Total Power

Leakage

NTV for Energy Efficiency

Source: Shekhar Borkar, Intel
NTV and Variability

Variability becomes worse at NTV

\[ \text{frequency} \propto \left( \frac{V_{dd} - V_t}{V_{dd}} \right)^\alpha \]

Source: Shekhar Borkar, Intel
Interconnect scaling: E-field increases

40nm pitch & 100B+ interconnects

- E field increases, and so do the number of interconnects
- Cu Migration & Dielectric failures specially with ULow-K ILD and linear defects are concerns

Source: Jose Maiz, Intel
Soft Errors: Cache cell

Cache Cell SEU Trend

SEU/Bit (a.u.)

Technology (nm)

180 130 90 65 45

neutron

total

α

Multi-Bit upset Probability

Probability

Cell to cell distance (μm)

Decreasing cell to cell distance increases probability of multi-bit upset

SER per bit is decreasing but...
Number of memory bits can double

Source: Jose Maiz, Intel
Soft Errors: Latch and System

SER per latch bit is decreasing but...
Number of latches double

SER for cache remains ~ constant
But SER for chip logic continues to increase because SER/latch is not decreasing fast enough

Source: Jose Maiz, Intel
Road to Unreliability?

_Pessimistic speculation, please do not use as data_

**Will this happen?**

Source: Shekhar Borkar, Intel
### Faults, Effects, and Measures

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<tr>
<th>Type of Fault</th>
<th>Effect</th>
<th>Measure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Permanent faults</td>
<td>Fan, power supply, shorts and opens</td>
<td>Sensors for detection Recover, reconfigure</td>
</tr>
<tr>
<td>Gradual spatial faults</td>
<td>Variations in frequency of cores</td>
<td>Screening, configuration</td>
</tr>
<tr>
<td>Gradual temporal faults</td>
<td>Temperature increase causing frequency loss</td>
<td>Detect and correct, proactively reconfigure</td>
</tr>
<tr>
<td>Intermittent faults</td>
<td>Data corruption by noise or soft error, control loss</td>
<td>Diagnose, retry, recover</td>
</tr>
<tr>
<td>Slow degradation</td>
<td>Frequency loss Erratic bits in memory</td>
<td>Proactive measure, testing, decommission faulty HW</td>
</tr>
</tbody>
</table>

Resiliency best implemented as **SW and HW Co-design**
Resiliency Framework for NFV

- Open Stack
- Open Stack/Open Day Light
- Open ??

At Application level:
  - Application aware
  - Redundancy and HA mechanisms

At VNF layer:
  - VNF state and network function connectivity persistence

At VM layer:
  - VM memory state, peripherals and connections persistence

At NFVI layer:
  - CPU, Bus and Memory sparing
  - device and connections mirroring or bonding

Failure detection & recovery at lower layers to contain faults propagation to upper layers reducing the system overhead

Predictive Failure Analysis to catch failures before they occur and allow system to take actions to provide HA
Summary

Integration and NFV consolidation drive resiliency challenges

Must understand and characterize faults

SW and HW Co-design is the most effective way to achieve resilient system

Detect errors in HW, diagnose & correct via SW

Solutions should be autonomous

Solutions must incur low cost, performance and power impact

System ‘Health’ Monitoring and Failure Prediction are the fundamental Resiliency Toolkit for NFV